IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:		)	
		)	
Appl. No.	: 10/823,970	)	Confirmation No. 5318
Applicant	: OGAWA, et al.	)	
Filed	: 13 April 2004	)	
Art Unit	: 2892	)	
Examiner	: Hoang, Quoc Dinh	)	
Attorney		)	
Docket No.	: SPSN-AF01215	)	
		)	
For: SEMICONDUCTOR DEVICE HAVING A PAD METAL LAYER AND A LOWER METAL LAYER THAT ARE ELECTRICALLY COUPLED, WHEREAS APERTURES ARE FORMED IN THE LOWER METAL LAYER BELOW A CENTER AREA OF THE PAD METAL LAYER		)	

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AND RESPONSE AND RCE

Dear Sir:

In response to the final Office Action dated April 9, 2009, and coincident with the RCE filed herewith, Applicants respectfully request reconsideration of the above-identified patent application. Please consider the following amendments and remarks for allowance of the above-identified patent application.

I hereby certify that this correspondence is being electronically transmitted to the USPTO via EFS on the date shown below:
June 16, 2009
/Christina Holland/
Christina Holland

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1. (currently amended) A semiconductor device comprising:

a pad metal layer having a perimeter area and a center area wherein said center area is formed to accommodate a probe;

a lower metal layer having a plurality of apertures below said center area of said pad metal layer, wherein said apertures are arranged into a plurality of rows each row comprising more than one of said apertures and a plurality of columns each column comprising more than one of said apertures;

an interlayer dielectric formed between said pad metal layer and said lower metal layer wherein said interlayer dielectric covers a portion of both the bottom and the sides of said pad metal layer;

a plurality of vias formed in said interlayer dielectric, wherein said plurality of vias electrically couple said pad metal layer and said lower metal layer, and wherein said plurality of vias form a ring arrangement that is located above and outside of the region occupied by said apertures in said lower metal layer and below an outermost perimeter area of said pad metal layer; and

an insulating dielectric layer that covers said perimeter area of said pad metal layer wherein said insulating dielectric layer covers a portion of both the top and the sides of said pad metal layer and extends in the direction of said center area laterally

inside of the innermost perimeter of said plurality of vias with said area inside of said innermost perimeter being free of vias.

2. (cancelled)

3. (previously presented) The semiconductor device as recited in Claim 1 wherein said vias are filled with tungsten.

4. (cancelled)

5. (cancelled)

6. (original) The semiconductor device as recited in Claim 1 wherein a probing process is performed on said center area of said pad metal layer.

7. (original) The semiconductor device as recited in Claim 1 wherein a wire-bonding process is performed on said center area of said pad metal layer.

8. (original) The semiconductor device as recited in Claim 1 wherein said semiconductor device is an integrated chip.

9.-15. (cancelled)

16. (withdrawn) A method of electrically coupling a pad metal layer and a lower metal layer in a semiconductor device, said method comprising:

forming a plurality of apertures in said lower metal layer, wherein said pad metal layer has a perimeter area and a center area, and wherein said apertures are located below said center area of said pad metal layer;

forming a plurality of vias in an interlayer dielectric between said pad metal layer and said lower metal layer, and wherein said vias are located below said perimeter area of said pad metal layer; and

filling said vias with a metal.

17. (withdrawn) The method as recited in Claim 16 wherein said metal is tungsten.

18. (withdrawn) The method as recited in Claim 16 wherein said vias are positioned in a ring arrangement below said pad metal layer.

19. (withdrawn) The method as recited in Claim 16 further comprising forming an insulating dielectric layer that covers said perimeter area of said pad metal layer.

20. (withdrawn) The method as recited in Claim 16 further comprising performing a probing process on said center area of said pad metal layer.

21. (withdrawn) The method as recited in Claim 16 further comprising performing a wire-bonding process on said center area of said pad metal layer.

22. (withdrawn) The method as recited in Claim 16 wherein said semiconductor device is an integrated circuit chip.

REMARKS

Claims 1, 3, 6-8 and 16-22 are pending in the instant patent application. Claim 1 is amended herein. Claims 2, 4, 5 and 9-15 were previously cancelled. Claims 16-22 have been withdrawn from consideration. Applicants respectfully request reconsideration of the instant application and pending Claims.

103 Rejection

Claims 1, 3 and 6-8 are rejected under 35 U.S.C. 103(b) as being unpatentable over Tanaka (US Patent No. 6,756,675) in view of AAPA in view of Lin et al. (US Patent No. 6,765,228). Applicants have reviewed the cited references and respectfully submit that the embodiments of the claimed invention that are set forth in Claims 1, 3 and 6-8 are not anticipated or rendered obvious by Tanaka in view of AAPA in view of Lin et al.

The Examiner is respectfully directed to independent Claim 1 which is drawn to a semiconductor device. Claim 1 is reproduced in its entirety below for convenience of the Examiner.

> 1. A semiconductor device comprising:
>
> a pad metal layer having a perimeter area and a center area;
>
> a lower metal layer having a plurality of apertures below said center area of said pad metal layer, wherein said apertures are arranged into a plurality of rows each row comprising more than one of said apertures and a plurality of columns each column comprising more than one of said apertures;
>
> an interlayer dielectric formed between said pad metal layer and said lower metal layer wherein said interlayer dielectric covers a portion of both the bottom and the sides of said pad metal layer;
>
> a plurality of vias formed in said interlayer dielectric, wherein said plurality of vias electrically couple said pad metal layer and said lower metal layer, and wherein said plurality of vias form a ring arrangement that is located above and outside of the region occupied by said apertures in said lower metal layer and below an outermost perimeter area of said pad metal layer; and
>
> an insulating dielectric layer that covers said perimeter area of said pad metal layer wherein said insulating dielectric layer covers a portion of both the top and the sides of said pad metal layer and extends in the direction of said

center area laterally inside of the innermost perimeter of said plurality of vias with said area inside of said innermost perimeter being free of vias. (emphasis added)

Claims 3 and 6-8 depend from Claim 1 and recite additional limitations of embodiments of the claimed invention.

Tanaka in view of AAPA in view of Lin et al. is deficient as Tanaka does not teach or suggest all of the limitations of Claim 1 and AAPA and Lin et al. does not remedy the deficiencies of Tanaka. In particular, Tanaka does not teach or suggest a semiconductor device that includes an insulating dielectric layer and an interlayer dielectric that has a plurality of vias formed therein that is formed between a pad metal layer and a lower metal layer, "wherein said insulating dielectric layer covers a portion of both the top and the sides of said pad metal layer and extends in the direction of said center area laterally inside of the innermost perimeter of said plurality of vias with said area inside of said innermost perimeter being free of vias" as is recited in Claim 1 (upon which Claims 3, 6 and 8 depend). Furthermore, AAPA and Lin et al. do not teach or suggest modifying Tanaka in a manner that remedies the above noted deficiencies of Tanaka.

Claim 1 has been amended to positively delimit that the recited insulating dielectric layer extends in the direction of said center area to the inside of the recited plurality of vias with the area inside of said innermost perimeter being free of vias. Support for the newly added limitations can be found in Applicants' drawings (see Figure 2). It should be appreciated that these limitations (along with the others recited in the

Claims) must be taught or suggested by the cited reference in order for a proper prima facie case to be supported thereby. However, Applicants respectfully submit that the newly added limitations are not taught or suggested anywhere by Tanaka in view of AAPA and Lin et al. If a rejection based on Tanaka in view of AAPA and Lin et al. is maintained, Applicants respectfully request that the parts of these references relied upon to teach the recited limitations be designated and clearly explained in accordance with MPEP 706 and 37 CFR 1.104(c)3.

In the outstanding final Office Action, in the "response to arguments" section, the examiner alleges that structures 612, 614, 616 and 618 teach the recited innermost vias of Applicants Claims. Applicants respectfully disagree. Assuming arguendo that structures 612, 614 and 618 could be considered innermost vias, Applicants' claims would still not be taught or suggested because the area inside of these structures is not free of vias as is required to meet the limitations of Claim 1. Accordingly, structures 612, 614, 616 and 618 clearly cannot be reasonably considered to teach the recited vias of Claim 1.

AAPA does not teach or suggest a modification of Tanaka that that would remedy the deficiencies of Tanaka discussed above. In particular, AAPA does not teach or suggest a semiconductor device that includes an insulating dielectric layer and an interlayer dielectric that has a plurality of vias formed therein that is formed between a pad metal layer and a lower metal layer, "wherein said insulating dielectric layer covers a portion of both the top and the sides of said pad metal layer and extends in the direction of said center area laterally inside of the innermost perimeter of said plurality of vias with

the area inside of said innermost perimeter being free of vias" as is recited in Claim 1 (upon which Claims 3, 6 and 8 depend). As it regards AAPA, Figure 1 clearly shows an insulating dielectric layer that does not extend in the direction of a center area laterally inside of the innermost perimeter of the plurality of vias. In fact, referring to Figure 1, the insulating dielectric layer does not even extend to the outermost perimeter of the plurality of vias. Accordingly, AAPA cannot reasonably be considered to teach or suggest a modification of Tanaka that would remedy the deficiencies of Tanaka discussed above.

Lin et al. does not teach or suggest a modification of Tanaka and AAPA that would remedy the deficiencies of Tanaka and AAPA discussed above. In particular, Lin et al. does not teach or suggest a semiconductor device that includes an insulating dielectric layer and an interlayer dielectric that has a plurality of vias formed therein which is formed between a pad metal layer and a lower metal layer, "wherein said insulating dielectric layer covers a portion of both the top and the sides of said pad metal layer and extends in the direction of said center area laterally inside of the innermost perimeter of said plurality of vias with said area inside of said innermost perimeter being free of vias" as is recited in Claim 1 (upon which Claims 3, 6 and 8 depend).

As understood by Applicants, Lin et al. shows a bonding pad with separate bonding and probing areas. Applicants respectfully submit that the device that is disclosed by Lin et al. is very dissimilar to claimed embodiments of Applicants' invention. Lin et al. is concerned with accommodating the probing of a semiconductor device in an area of the semiconductor device that is different from the area of the

semiconductor device in which bonding is effected. Lin et al. discloses that this is accomplished by designating portions of an elongated, rectangular bonding pad for each of the aforementioned purposes (see Abstract). However, Lin et al. does not teach or suggest an insulating dielectric layer that extends in the direction of said center area laterally inside of the innermost perimeter of a plurality of vias with said area inside of said innermost perimeter being free of vias as recited in Applicants' Claim 1. In fact, Lin et al. does not teach an insulating dielectric layer at all. Accordingly, Lin et al. cannot reasonably be considered to teach or suggest a modification of Tanaka that would remedy the deficiencies of Tanaka discussed above.

Based on Applicants' aforementioned review of Tanaka, AAPA and Lin et al., Applicants respectively submit that nowhere therein is a semiconductor device taught or suggested that includes an insulating dielectric layer and an interlayer dielectric that has a plurality of vias formed therein that is formed between a pad metal layer and a lower metal layer, "wherein said insulating dielectric layer covers a portion of both the top and the sides of said pad metal layer and extends in the direction of said center area laterally inside of the innermost perimeter of said plurality of vias with said area inside of said innermost perimeter being free of vias" as is recited in Claim 1 (upon which Claims 3, 6 and 8 depend). Consequently, as alluded to above, Tanaka in view of AAPA and Lin et al. fails to teach or suggest all of the limitations recited in Claim 1.

With regard to Claim 6, Applicants respectfully submit that nowhere in the Tanaka, AAPA and Lin et al. references is a semiconductor device taught or suggested

that includes as features the above discussed limitations of Claim 1 and further includes as features the limitations "wherein a probing process is performed on said center area of said pad metal layer" as are set forth in Claim 6. With regard to Claim 7, Applicants respectfully submit that nowhere in the Tanaka, AAPA and Lin et al. references is a semiconductor device taught or suggested that includes as features the above discussed limitations of Claim 1 and further includes as features the limitations "wherein a wire-bonding process is performed on said center area of said pad metal layer" as are set forth in Claim 7. With regard to Claim 8, Applicants respectfully submit that nowhere in the Tanaka, AAPA and Lin et al. references is a semiconductor device taught or suggested that includes as features the above discussed limitations of Claim 1 and further includes as features the limitations "wherein said semiconductor device is an integrated chip" as are set forth in Claim 8 taught or suggested.

Because of deficiencies of Tanaka, AAPA and Lin et al. discussed above, Applicants respectfully submit that Tanaka in view of AAPA and Lin et al. does not provide an adequate basis for rejection of Claim 1 under 35 U.S.C. §103 and, as such, Claim 1 is allowable. Accordingly, the Applicants respectfully submit that Claims 3 and 6-8 dependent on Claim 1 are likewise allowable at least as being dependent on allowable base claims.

CONCLUSION

For at least the above provided reasons, it is respectfully submitted that all remaining claims are in condition for allowance.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

Murabito, Hao & Barnes LLP

Date: June 16th, 2009

/James P. Hao/

James P. Hao
Reg. No.: 36,398
Two North Market Street
Third Floor
San Jose, California 95113